

WHAT IS CLAIMED IS:

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- 1. A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit, comprising the steps of:
 - (A) attaching at least a part of a first surface of said semiconductor unit to a carrier; and
 - (B) etching said semiconductor unit from a second surface of said semiconductor unit until the size of said semiconductor unit meets an expected specification.
- 2. The method according to claim 1 wherein said semiconductor unit is etched by means selected from among using gas and using beams of light.
 - 3. The method according to claim 1 wherein said semiconductor unit is etched by using plasma.
- 4. The method according to claim 1 wherein said expected specification means that the thickness of said semiconductor unit measured relative to said first surface is within a specified range.

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- The method according to claim 4 wherein said specified range is the range spanning between 2 mil and 6 mil.
- 6. The method according to claim 1 wherein step (B) comprises a step of shielding at least a part of said semiconductor unit and said carrier to prevent said etching from affecting the quality of said semiconductor unit and said carrier.
 - 7. The method according to claim 1 further comprising, before step (A), a step of grinding said semiconductor unit until the size thereof approximates said expected specification.
 - 8. The method according to claim 1 wherein step (B) comprises a step of using a fixture to shield at least a part of said semiconductor unit and said carrier for preventing said etching from affecting the quality

of said semiconductor unit and said carrier.

9. The method according to claim 1 wherein said semiconductor unit is attached to said carrier according to a configuration selected from among bump connection and lead-on chip packaging.

- 10. The method according to claim 1 wherein said carrier is selected from among a chip tray and a chip carrier, and said semiconductor unit includes at least a semiconductor electrical connection device located on said first surface.
- 11. A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface, a second surface, and at least a semiconductor electrical connection device located on said first surface, said method comprising the steps of:
 - (A) attaching said semiconductor unit to a seating apparatus, with said first surface facing said seating apparatus and said second surface exposed; and
 - (B) etching said semiconductor unit from said second surface until the size of said semiconductor unit meets an expected specification.
- 12. The method according to claim 11 wherein said semiconductor unit is etched by means selected from among using gas, beams of light, and plasma.
 - 13. The method according to claim 11 further comprising, before step (A), a step of grinding said semiconductor unit until the size of said semiconductor unit approximates said expected specification.
 - 14. The method according to claim 11 wherein said seating apparatus is selected from among a chip tray, and a chip carrier connectible with said semiconductor unit; and wherein said expected specification means that the thickness of said semiconductor unit measured

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relative to said first surface is within a specified range.

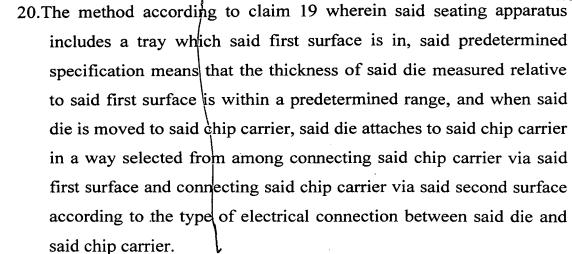
- 15. The method according to claim 11 wherein said first surface is prevented by said seating apparatus from being etched.
- 16. The method according to claim 11 further comprising a step of moving said semiconductor unit from said seating apparatus to a carrier with said second surface attaching to said carrier via adhesive material.
- 17. The method according to claim 11 further comprising a step of moving said semiconductor unit from said seating apparatus to a carrier with said first surface attaching to said carrier via at least a bump.
- 18. The method according to claim 11 further comprising a step of moving said semiconductor unit from said seating apparatus to a carrier for forming a lead-on chip package.
- 19. A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface, a second surface, and at least a semiconductor electrical connection device located on said first surface, said method comprising the steps of:

dividing a wafer into a plurality of dice;

placing at least one die of said dice onto a seating apparatus, with said second surface exposed;

etching said die from said second surface, with said first surface shielded by said seating apparatus and thereby immunized against etching;

ending etching said die when the size of said die meets a predetermined specification, and moving said die from said seating apparatus to a chip carrier.



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